

**ELECTRONIC DEVICES INCLUDING ELECTRODES WITH
INSULATING SPACERS THEREON AND RELATED METHODS**

RELATED APPLICATIONS

[0001] The present application claims the benefit of priority from Korean Application No. P2003-0081099 filed November 7, 2003, the disclosure of which is hereby incorporated herein in its entirety by reference.

FIELD OF THE INVENTION

[0002] The present invention relates to the field of electronics and more particularly to electrodes for electronic devices and related methods.

BACKGROUND

[0003] As dynamic random access memory (DRAM) devices become more highly integrated, the area available for each memory cell is reduced. Accordingly, the substrate area available for each memory cell capacitor may be reduced so that it may be difficult to maintain a desired memory cell capacitance as integration densities increase. Reduced memory cell capacitances may increase a soft error rate (SER), degrade memory cell operation at low voltages, and/or result in more frequent memory refresh operations. Accordingly, there exists a need to provide a memory cell capacitor occupying a reduced surface area of the memory device substrate while maintaining a desired capacitance.

[0004] In response, capacitors having three-dimensional structures have been proposed to increase the surface area of the capacitor electrodes thereby increasing the capacitance of the resulting capacitor. In particular, cylindrical electrode structures may be used where inner and outer surfaces of a cylinder are used to increase an effective capacitor electrode area. A surface area of a cylindrical capacitor electrode structure may be further increased by increasing a height of the structure.

[0005] A cylindrical electrode structure may be formed, for example, as shown in Figures 6A-B. As shown in Figure 6A, an insulating layer 701 and an etch stopping layer 703 may be formed on a substrate 700, and conductive plugs 702 may provide electrical coupling through the etch stopping and insulating layers 703 and 701. A first sacrificial layer 704 may be formed on the etch stopping layer 703, and holes through the first sacrificial layer 704 may expose the conductive plugs 702. Cylindrical electrodes 705 may be formed on sidewalls of the holes in the first sacrificial layer 704, and a second sacrificial layer 706 may be provided within the cylindrical electrodes.

[0006] The sacrificial layers 704 and 706 may be removed as shown in Figure 6B so that inside and outside surfaces of the cylindrical electrodes 705 are exposed, and a capacitor dielectric layer and a second capacitor electrode may be formed on the exposed surfaces of the cylindrical electrodes 705. With relatively tall and/or closely packed cylindrical electrode structures, however, adjacent cylindrical electrodes may lean together once the support provided by the sacrificial layers is removed. As shown in Figure 6B, an electrical short may thus result between adjacent cylindrical electrodes at 707 prior to forming a capacitor dielectric layer. For example, cylindrical electrodes may lean together while being cleaned and/or dried after removing the sacrificial layers.

SUMMARY

[0007] According to embodiments of the present invention, an electronic device may include a substrate, a conductive electrode on the substrate, and a conductive spacer. The conductive electrode may have an electrode wall extending away from the substrate, and the insulating spacer may be on the electrode wall with portions of the electrode wall being free of the insulating spacer between the substrate and the insulating spacer. In addition, portions of the electrode wall may extend from the insulating spacer away from the substrate free of the insulating spacer, and/or the electrode wall may include a recessed portion with the insulating spacer being on the recessed portion of the electrode wall.

[0008] Moreover, the electrode wall may be closed thereby defining an inside of the electrode wall and an outside of the electrode wall. For example, the electrode wall may define a cylinder. The device may also include a capacitor dielectric layer on portions of the conductive electrode free of the spacer, and a second conductive electrode on the capacitor dielectric layer opposite the first electrode. The spacer may have a first thickness separating the conductive electrodes, and the capacitor dielectric layer may have a second thickness separating the conductive electrodes with the first thickness being greater than the second thickness.

[0009] The substrate may also include a memory cell access transistor, and the conductive electrode may be electrically coupled with a source/drain region of the memory cell access transistor. In addition, a sacrificial layer may have a thickness on the substrate such that the sacrificial layer extends to the insulating spacer, and the sacrificial layer and the insulating spacer may comprise different materials.

[0010] According to additional embodiments of the present invention, a conductive electrode may be formed on a substrate, and the conductive electrode may include an electrode wall extending away from the substrate. An insulating spacer may be formed on the electrode wall wherein portions of the electrode wall are free of the insulating spacer between the substrate and the insulating spacer. In addition, portions of the electrode wall may extend from the insulating spacer away from the substrate free of the insulating spacer.

[0011] The electrode wall may also include a recessed portion, and the insulating spacer may be formed on the recessed portion of the electrode wall. Moreover, the recessed portion of the electrode wall may extend from the insulating spacer away from the substrate free of the insulating spacer.

[0012] A capacitor dielectric layer may also be formed on portions of the conductive electrode free of the spacer, and a second conductive electrode may be formed on the capacitor dielectric layer opposite the first electrode. More particularly, the spacer may have a first thickness separating the conductive electrodes, the capacitor dielectric layer may have a second thickness separating

the conductive electrodes, and the first thickness may be greater than the second thickness. The electrode wall may be closed thereby defining an inside of the wall and an outside of the electrode wall. For example, the electrode wall may define a cylinder.

[0013] In addition, a sacrificial layer having a hole therein may be formed on the substrate, and forming the conductive electrode may include forming the electrode wall on a sidewall of the hole in the sacrificial layer. Portions of the sacrificial layer may be removed to expose a portion of the electrode wall while maintaining a portion of the sacrificial layer between the exposed portion of the electrode wall and the substrate. More particularly, the sacrificial layer and the insulating spacer may comprise different materials, and forming the insulating spacer may include forming the insulating spacer on the exposed portion of the electrode wall. Moreover, portions of the sacrificial layer between the insulating spacer and the substrate may be removed after forming the insulating spacer. Removing a portion of the sacrificial layer may include removing at least approximately 200Å of the sacrificial layer, and at least approximately 10,000Å of the sacrificial layer may remain after removing at least approximately 200Å of the sacrificial layer. Accordingly, a length of portions of the electrode between the substrate and the insulating spacer may be at least approximately 10,000Å.

[0014] The substrate may include a memory cell access transistor, and the conductive electrode may be electrically coupled with a source/drain region of the memory cell access transistor. In addition, a sacrificial layer may be formed on the substrate such that the sacrificial layer extends to the insulating spacer, and the sacrificial layer and the insulating spacer may comprise different materials.

[0015] According to still additional embodiments of the present invention, an electronic device may include a substrate and a conductive electrode on the substrate. More particularly, the conductive electrode may include an electrode wall extending away from the substrate, and the electrode wall may include a recessed portion at an end thereof opposite the substrate. In addition, an insulating spacer may be provided on the recessed portion of the electrode wall

with portions of the electrode wall being free of the insulating spacer between the substrate and the insulating spacer, and portions of the electrode wall may extend from the insulating spacer away from the substrate free of the insulating spacer.

[0016] The electrode wall may be closed thereby defining an inside of the electrode wall and an outside of the electrode wall. For example, the electrode wall may define a cylinder. In addition, a capacitor dielectric layer may be provided on portions of the conductive electrode, and a second conductive electrode may be provided on the capacitor dielectric layer opposite the first electrode. An insulating spacer may also be provided on the recessed portion of the electrode wall such that portions of the electrode wall are free of the insulating spacer between the substrate and the insulating spacer. Moreover, the spacer may have a first thickness separating the conductive electrodes, the capacitor dielectric layer may have a second thickness separating the conductive electrodes, and the first thickness may be greater than the second thickness.

[0017] The substrate may also include a memory cell access transistor, and the conductive electrode may be electrically coupled with a source/drain region of the memory cell access transistor. A sacrificial layer on the substrate may have a thickness such that the sacrificial layer extends to the recessed portion of the electrode wall, and the recessed portion of the electrode wall may be free of the sacrificial layer.

[0018] According to yet additional embodiments of the present invention, a method of forming an electronic device may include forming a conductive electrode on a substrate, and the conductive electrode may have an electrode wall extending away from the substrate. A recessed portion may be formed at an end of the electrode wall opposite the substrate.

[0019] Moreover, an insulating spacer may be formed on the recessed portion of the electrode wall, and portions of the electrode wall may be free of the insulating spacer between the substrate and the insulating spacer. In addition, portions of the electrode wall may extend from the insulating spacer away from the substrate free of the insulating spacer. More particularly, the recessed portion of

the electrode wall may extend from the insulating spacer away from the substrate free of the insulating spacer.

[0020] A capacitor dielectric layer may be formed on portions of the conductive electrode, and a second conductive electrode may be formed on the capacitor dielectric layer opposite the first electrode. In addition, an insulating spacer may be formed on the recessed portion of the electrode wall with portions of the electrode wall being free of the insulating spacer between the substrate and the insulating spacer. More particularly, the spacer may have a first thickness separating the conductive electrodes, the capacitor dielectric layer may have a second thickness separating the conductive electrodes, and the first thickness may be greater than the second thickness. The electrode wall may be closed thereby defining an inside of the wall and an outside of the electrode wall. For example, the electrode wall may define a cylinder.

[0021] A sacrificial layer having a hole therein may be formed on the substrate, and forming the conductive electrode may include forming the electrode wall on a sidewall of the hole in the sacrificial layer. In addition, a portion of the sacrificial layer may be removed before forming the recessed portion of the electrode wall to expose a portion of the electrode wall while maintaining a portion of the sacrificial layer between the exposed portion of the electrode wall and the substrate. More particularly, forming the recessed portion of the electrode wall may include forming the recessed portion of the electrode wall at portions of the electrode wall exposed by the sacrificial layer. An insulating spacer may also be formed on the recessed portion of the electrode wall wherein the sacrificial layer and the insulating spacer comprise different materials.

[0022] After forming the recessed portions of the electrode wall, a portion of the sacrificial layer between the recessed portions of the electrode wall and the substrate may be removed. Moreover, removing a portion of the sacrificial layer may include removing at least approximately 200Å of the sacrificial layer. More particularly, at least approximately 10,000Å of the sacrificial layer may remain after removing at least approximately 200Å of the sacrificial layer.

[0023] A length of portions of the electrode wall between the substrate and the recessed portion may be at least approximately 10,000Å. In addition, the substrate may include a memory cell access transistor, and the conductive electrode may be electrically coupled with a source/drain region of the memory cell access transistor.

BRIEF DESCRIPTION OF THE DRAWINGS

[0024] Figure 1 is a cross-sectional view of memory devices including capacitor electrodes according to embodiments of the present invention.

[0025] Figures 2A-F are cross-sectional views illustrating steps of forming electrodes according to embodiments of the present invention.

[0026] Figures 3A-F are cross-sectional views illustrating steps of forming electrodes according to additional embodiments of the present invention.

[0027] Figures 4A-B are cross-sectional views illustrating steps of forming electrodes according to yet additional embodiments of the present invention.

[0028] Figures 5A-B are cross-sectional views illustrating steps of forming electrodes according to still additional embodiments of the present invention.

[0029] Figure 6A-B are cross-sectional views illustrating steps of forming electrodes according to the prior art.

DETAILED DESCRIPTION

[0030] The present invention will now be described more fully with reference to the accompanying drawings, in which preferred embodiments of the invention are shown. This invention may, however, be embodied in many different forms and should not be construed as being limited to the embodiments set forth herein; rather, these embodiments are provided so that this disclosure will be thorough and complete, and will fully convey the concept of the invention to those skilled in the art. In the drawings, the size and the thickness of layers and regions are exaggerated for clarity. It will also be understood that when a layer is referred

to as being on another layer or substrate, it can be directly on the other layer or substrate, or intervening layers may also be present. It will also be understood that when a layer or element is referred to as being connected to or coupled to another layer or element, it can be directly connected to or coupled to the other layer or element, or intervening layers or elements may also be present.

[0031] According to embodiments of the present invention, an electronic device may include electrodes **101** having electrode walls **103** extending from a substrate **105** (such as a silicon substrate). In addition, insulating spacers **107** (such as silicon nitride and/or silicon oxynitride spacers) may be provided on the electrode walls **103** such that portions of the electrode walls are free of the insulating spacers **107** between the substrate **105** and the insulating spacers **107**. More particularly, an insulating layer **109** (such as a silicon oxide layer) may be provided between the capacitor electrodes **101** and the substrate **105**, and conductive plugs **111** (such as doped polysilicon plugs) may provide electrical coupling between the capacitor electrodes **101** and a surface of the substrate **105**.

[0032] By way of example, the capacitor electrodes **101** may be first electrodes of storage capacitors for a dynamic random access memory device. Moreover, the conductive plugs **111** may provide electrical connection between the electrodes **101** and source/drain regions **115** of memory cell access transistors. The memory cell access transistors may also include gate electrodes **117**, gate dielectric layers **119**, and second source/drain regions **121** (which may be coupled to a bit line(s) not illustrated in Figure 1). In addition, a capacitor dielectric layer(s) **131** may be provided on the first capacitor electrodes **101**, and second capacitor electrode(s) **133** may be provided on the capacitor dielectric layer(s) **131** opposite the first capacitor electrodes **101**. The electronic device may also include an etch-stopping layer **123** (such as a silicon nitride layer) between the insulating layer **109** and the electrodes **101**.

[0033] As shown in Figure 1, the spacers **107** may be provided on electrode walls **103** at ends of the electrode walls **103**. According to alternate embodiments, however, the electrode walls **103** may extend beyond the spacers. According to additional embodiments, recesses may be provided in the electrode

walls **103** adjacent the spacers **107** so that the spacers **107** on thinner portions of the electrode walls do not extend significantly beyond wider portion(s) of the electrode walls. The spacers **107** may reduce the possibility of shorting between first capacitor electrodes **101** if adjacent electrode walls **103** of different electrodes **101** lean together before formation of the capacitor dielectric layer **131** and/or the second capacitor electrode **133**. Moreover, spacers **107** could be provided on outside surfaces of the electrode walls **103** without being provided on inside surfaces of the electrode walls **103**.

[0034] Steps of fabricating electrodes according to embodiments of the present invention will now be discussed with reference to Figures 2A-F. As shown in Figure 2A, an insulating layer **201** (such as a silicon oxide layer) may be formed on substrate **200** (such as a silicon substrate), and an etch stopping layer **203** (such as a silicon nitride layer) may be formed on the insulating layer **201**. Openings may then be formed through the insulating and etch stopping layers **201** and **203**, and conductive plugs **202** (such as polysilicon plugs) may be formed in the openings to provide electrical connection through the insulating layer **201** and the etch stopping layer **203**. The conductive plugs **202**, for example, may be formed by depositing a polysilicon layer on the etch stopping layer **203** and in openings in the etch stopping layer **203** and the insulating layer **201**, and then etching and/or polishing back the polysilicon layer to expose portions of the etch stopping layer **203** while maintaining the polysilicon in the openings in the insulating layer **201**.

[0035] A first sacrificial layer **204** may be formed on the etch stopping layer **203** and on exposed portions of the conductive plugs **202**, and holes through the first sacrificial layer **204** may expose the conductive plugs **202**. The sacrificial layer, for example, may be a layer of a material(s) different than a material of the etch stopping layer **203** so that the first sacrificial layer **204** can be selectively removed without significantly removing the etch stopping layer **203**. More particularly, the first sacrificial layer **204** may be a layer of an insulating material such as silicon oxide and/or silicon oxynitride. Moreover, the first sacrificial layer may include two or more separately formed layers of the same or different materials.

[0036] A conductive layer 205 is then formed on the first sacrificial layer 204 including the holes therein and on the exposed portions of the conductive plugs 202. While not shown in Figure 2A, the holes in the first sacrificial layer may expose portions of the etch stopping layer 203 adjacent the conductive plugs 202 so that the conductive layer 205 may extend onto exposed portions of the etch stopping layer 203. More particularly, the conductive layer 205 may be a layer of polysilicon having a thickness of approximately 500Å (Angstroms). A second sacrificial layer 206 may then be formed on the conductive layer 205. The second sacrificial layer 206 may be a layer of an insulating material that can be selectively removed without significantly removing the conductive layer 205 and/or the etch stopping layer 203. While not required, the first and second sacrificial layers 204 and 206 may comprise a same material such as silicon oxide and/or silicon oxynitride.

[0037] As shown in Figure 2B, portions of the second sacrificial layer 206 and the conductive layer 205 (opposite the substrate) may be removed (such as by etching and/or polishing back) so that the first sacrificial layer 204 is exposed, and so that portions of the conductive layer 205 in the holes are electrically separated. Accordingly, the remaining portions of conductive layers 205 may define respective electrodes 205' including electrode walls (having outside surfaces 205a' and inside surfaces 205b') extending away from the substrate. Stated in other words, each electrode 205' may include a closed wall defining a cylinder.

[0038] Accordingly, the electrode wall outside surfaces 205a' may be formed along sidewalls of the holes in the first sacrificial layer 204, and electrode wall inside surfaces 205b' may be provided along the second sacrificial layer 206'. A geometry of the electrode wall outside surfaces 205a' can thus be defined by the sidewalls of the holes in the first sacrificial layer 204. Accordingly, a hole in the first sacrificial layer having a circular profile may provide an electrode wall outside surface 205a' having a cylindrical profile. As used herein, the term "cylindrical" may include a shape of an electrode wall outside surface 205a' that may result when formed in a circular hole having sloped sidewalls such as may result when an isotropic etch is used to form the holes in the first sacrificial layer

204. Electrodes having other shapes may be provided, for example, by providing holes with different profiles (such as square or rectangular) in the first sacrificial layer.

[0039] After removing portions of the second sacrificial layer **206** and the conductive layer **205** as shown in Figure 2B, the remaining portions of the first sacrificial layer **204** may have a thickness of 20,000Å or greater. A length of the electrode wall outside surface **205a'** may be determined by the thickness of the first sacrificial layer **204** remaining in Figure 2B. Moreover, portions of the first sacrificial layer **204** may be removed when removing portions of the second sacrificial layer **206** and the conductive layer **205**, so that a thickness of the first sacrificial layer **204** in Figure 2B is less than a thickness of the first sacrificial layer **204** in Figure 2A. In addition, a thickness of the electrode **205'** (between the outside surface **205a'** and inside surface **205b'**) of Figure 2B may be determined by a thickness of the conductive layer **205** of Figure 2A.

[0040] In Figure 2C, portions of the first sacrificial layer **204** and the second sacrificial layer **206** are removed selectively with respect to the electrodes **205'**. Accordingly, portions of the electrodes **205'** may extend beyond the first and second sacrificial layers **204** and **206**. For example, 200Å to 500Å of the first and second sacrificial layers **204** and **206** may be removed so that 200Å to 500Å of the outside and inside surfaces **205a'** and **205b'** of the electrode walls are exposed. The sacrificial layers **204** and **206** may be removed, for example, using a buffered oxide etch (BOE) such as a low ammoniumfluoride liquid (LAL) chemical etch. An LAL etch, for example, may include 2.5 Wt.% HF, 17 Wt.% NH₄F, 80.5 Wt.% de-ionized (DI) water, and 400 ppm surfactant.

[0041] As shown in Figure 2D, an insulating layer **208** may be formed on the exposed portions of the electrodes **205'** and on the first and second sacrificial layers **204** and **206**. The insulating layer **208** may be a layer of a material (such as silicon nitride) different than that used for the first and second sacrificial layers **204** and **206** so that the insulating layer **208** may be removed selectively with respect to the first and second sacrificial layers and so that the first and second sacrificial layers **204** and **206** can be removed selectively with respect

to the insulating layer 208. The insulating layer 208 can then be subjected to an anisotropic etch to form spacers 208' as shown in Figure 2E. In particular, the anisotropic etch may be performed for a period of time sufficient to expose portions of the first and second sacrificial layers 204 and 206 while maintaining portions of the insulating layer 208 on the exposed inside and outside surfaces 205a' and 205b' of the electrode walls to provide spacers 208' as shown.

[0042] The first and second sacrificial layers 204 and 206 can then be removed as shown in Figure 2F. More particularly, an etch chemistry may be selected so that the first and second sacrificial layers 204 and 206 are removed selectively with respect to the spacers 208', the electrodes 205', and the etch stopping layer 203. The electrodes 205' may thus be provided with spacers 208' at or near ends thereof. Accordingly, the electrodes 205' may lean together without electrically shorting. The sacrificial layers may be removed using a buffered oxide etch (BOE) such as an LAL chemical etch as discussed above.

[0043] A capacitor dielectric layer may then be formed on exposed portions of the electrodes 205', and a second capacitor electrode may be formed on the capacitor dielectric layer opposite the first electrodes 205'. For example, the capacitor dielectric layer may be a layer of a dielectric material such as silicon oxide (SiO₂) and/or aluminum oxide (Al₂O₃) having a thickness in the range of approximately 30Å to 50Å. The capacitor dielectric layer, for example, may be formed by chemical vapor deposition and/or atomic layer deposition. Electrodes 205' of Figure 2F may thus be used to provide first capacitor electrodes of dynamic random access memory cells. More particularly, the substrate 200 may include respective memory cell access transistors coupled to each of the electrodes 205', and the memory cell access transistors may provide coupling between the electrodes 205' and respective bit lines responsive to read/write signals provided on respective word lines.

[0044] Steps of fabricating electrodes according to additional embodiments of the present invention will now be discussed with reference to Figures 3A-F. As shown in Figure 3A, an insulating layer 401 (such as a silicon oxide layer) may be formed on substrate 400 (such as a silicon substrate), and an

etch stopping layer 403 (such as a silicon nitride layer) may be formed on the insulating layer 401. Openings may then be formed through the insulating and etch stopping layers 401 and 403, and conductive plugs 402 (such as polysilicon plugs) may be formed in the openings to provide electrical connection through the insulating layer 401 and the etch stopping layer 403. The conductive plugs 402, for example, may be formed by depositing a polysilicon layer in openings in the etch stopping layer 403 and the insulating layer 401, and then etching and/or polishing back the polysilicon layer to expose portions of the etch stopping layer while maintaining the polysilicon in the openings in the insulating layer.

[0045] A first sacrificial layer 404 may be formed on the etch stopping layer 403 and on exposed portions of the conductive plugs 402, and holes through the first sacrificial layer 404 may expose the conductive plugs 402. The sacrificial layer 404, for example, may be a layer of a material(s) different than a material of the etch stopping layer 403 so that the first sacrificial layer 404 can be selectively removed without significantly removing the etch stopping layer 403. More particularly, the first sacrificial layer 404 may be a layer of an insulating material such as silicon oxide and/or silicon oxynitride. Moreover, the first sacrificial layer 404 may include two or more separately formed layers of the same or different materials.

[0046] A conductive layer is then formed on the first sacrificial layer 404 including the holes therein and on the exposed portions of the conductive plugs 402. While not shown in Figure 3A, the holes in the first sacrificial layer may expose portions of the etch stopping layer 403 adjacent the conductive plugs 402 so that the conductive layer may extend onto exposed portions of the etch stopping layer 403. More particularly, the conductive layer may be a layer of polysilicon having a thickness of approximately 500Å. A second sacrificial layer 406 may then be formed on the conductive layer. The second sacrificial layer 406 may be a layer of an insulating material that can be selectively removed without significantly removing the conductive layer and/or the etch stopping layer 403. While not required, the first and second sacrificial layers 404 and 406 may comprise a same material such as silicon oxide and/or silicon oxynitride.

[0047] As further shown in Figure 3A, portions of the second sacrificial layer 406 and the conductive layer (opposite the substrate) may be removed (such as by etching and/or polishing back) so that the first sacrificial layer 404 is exposed, and so that portions of the conductive layer in the holes are electrically separated. Accordingly, the remaining portions of the conductive layer may define respective electrodes 405' each including an electrode wall(s) having an outside surface 405a' and an inside surface 405b' extending away from the substrate. Stated in other words, each electrode 405' may be closed so that each electrode wall defines a cylinder. The structure of Figure 3A may thus be equivalent to that of Figure 2B.

[0048] Accordingly, the electrode wall outside surfaces 405a' may be formed along sidewalls of the holes in the first sacrificial layer 404, and the second sacrificial layer 406' may be provided along electrode wall inside surfaces 405b'. A geometry of the electrode wall outside surfaces 405a' can thus be defined by the sidewalls of the holes in the first sacrificial layer 404. Accordingly, a hole in the first sacrificial layer having a circular profile may provide an electrode wall outside surface 405a' having a cylindrical profile. As used herein, the term "cylindrical" may include a shape of an electrode wall outside surface 405a' that may result when formed in a hole having sloped sidewalls such as may result when an isotropic etch is used to form the holes in the first sacrificial layer 404. Electrodes having other shapes may be provided, for example, by providing holes with different profiles (such as square or rectangular) in the first sacrificial layer.

[0049] After removing portions of the second sacrificial layer 406 and the conductive layer 405 as shown in Figure 3B, the remaining portions of the first sacrificial layer 404 may have a thickness of 20,000Å or greater. A length of the electrode wall outside surfaces 405a' may be determined by the thickness of the first sacrificial layer 404 remaining in Figure 3B. Moreover, portions of the first sacrificial layer 404 may be removed when removing portions of the second sacrificial layer 406 and the conductive layer 405, so that a thickness of the first sacrificial layer 404 in Figure 3A is less than a thickness of the originally formed first sacrificial layer 404 in Figure 3A. In addition, a thickness of the electrode

405' (between the outside surface **405a'** and inside surface **405b'**) of Figure 3A may be determined by a thickness of the originally formed conductive layer, such as discussed above with respect to Figures 2A-B.

[0050] In Figure 3B, portions of the first sacrificial layer **404** and the second sacrificial layer **406** are removed selectively with respect to the electrodes **405'**. Accordingly, portions of the electrodes **405'** may extend beyond the first and second sacrificial layers **404** and **406**. For example, 200Å to 500Å of the first and second sacrificial layers **404** and **405** may be removed so that 200Å to 500Å of the outside and inside surfaces **405a'** and **405b'** of the electrode walls are exposed. The sacrificial layers **404** and **406** may be removed, for example, using a buffered oxide etch (BOE) such as a low ammoniumfluoride liquid (LAL) chemical etch. An LAL etch, for example, may include 2.5 Wt.% HF, 17 Wt.% NH₄F, 80.5 Wt.% de-ionized (DI) water, and 400 ppm surfactant.

[0051] Portions of the electrode wall inside and outside surfaces **405a'** and **405b'** exposed by removing portions of the sacrificial layers **404** and **406** may then be etched to provide recessed portions of the electrode walls. For example, an isotropic etch may be used that removes the conductive material of the electrodes **405'** selectively with respect to the first and second sacrificial layers **404** and **406**. More particularly, approximately 150Å of the exposed portions of the electrodes **405'** may be removed so that exposed portions of the electrodes **405'** are recessed (at **421**, for example) with respect to portions of the electrode **405'** protected by the first and second sacrificial layers **404** and **406**. Portions of the electrodes **405'** protected by the sacrificial layers **404** and **406** may thus maintain a thickness of approximately 500Å while portions of the electrodes **405'** extending beyond the sacrificial layers **404** and **406** may be thinned to approximately 200Å, as shown in Figure 3C.

[0052] As shown in Figure 3D, an insulating layer **408** may be formed on the recessed portions of the electrodes **405'** and on the first and second sacrificial layers **404** and **406**. The insulating layer **408** may be a layer of a material (such as silicon nitride) different than that used for the first and second sacrificial layers **404** and **406** so that the insulating layer **408** may be removed

selectively with respect to the first and second sacrificial layers and so that the first and second sacrificial layers 404 and 406 can be removed selectively with respect to the insulating layer 408. The insulating layer 408 can then be subjected to an anisotropic etch to form spacers 408' as shown in Figure 3E. In particular, the anisotropic etch may be performed for a period of time sufficient to expose portions of the first and second sacrificial layers 404 and 406 while maintaining portions of the insulating layer 408 on the recessed portions of the electrode wall inside and outside surfaces 405a' and 405b' to provide spacers 408'.

[0053] The first and second sacrificial layers 404 and 406 can then be removed as shown in Figure 3F. More particularly, an etch chemistry may be selected so that the first and second sacrificial layers 404 and 406 are removed selectively with respect to the spacers 408', the electrodes 405', and the etch stopping layer 403. The sacrificial layers may be removed using a buffered oxide etch (BOE) such as an LAL chemical etch as discussed above.

[0054] The electrodes 405' may thus be provided with spacers 408' on recessed portions of the electrode wall inside and outside surfaces 405a' and 405b' at or near ends thereof. Accordingly, the electrodes 405' may lean together without electrically shorting. By providing the spacers 408' on recessed portions of the electrodes 405', shadowing of portions of the electrodes 405' (between the spacers and the substrate) may be reduced during subsequent processing steps. Accordingly, subsequent uniformity of depositions (such as depositions of a capacitor dielectric layer and/or a second capacitor electrode) on portions of the electrodes 405' between the spacers 408' and the etch stopping layer 403 may be improved.

[0055] A capacitor dielectric layer may then be formed on exposed portions of the electrodes 405', and a second capacitor electrode may be formed on the capacitor dielectric layer opposite the first electrodes 405'. For example, the capacitor dielectric layer may be a layer of a dielectric material such as silicon oxide (SiO₂) and/or aluminum oxide (Al₂O₃) having a thickness in the range of approximately 30Å to 50Å. The capacitor dielectric layer, for example, may be formed by chemical vapor deposition and/or atomic layer deposition. Uniformity

of capacitor dielectric layers and/or second capacitor electrodes formed on electrodes **405'** of Figure 3F may thus be improved by providing the spacers **408'** on recessed (thinned) portions of the electrodes **405'**.

[0056] Electrodes **405'** of Figure 3F may thus be used to provide first capacitor electrodes of dynamic random access memory cells. More particularly, the substrate **400** may include respective memory cell access transistors coupled to each of the electrodes **405'**, and the memory cell access transistors may provide coupling between the first electrodes **405'** and respective bit lines responsive to read/write signals provided on respective word lines.

[0057] Steps of forming electrodes according to still additional embodiments of the present invention are illustrated in Figures 4A-B. The structure illustrated in Figure 4A can be formed according to steps similar to those discussed above with respect to Figures 2A-B, with a difference being that a greater thickness of the sacrificial layers **504** and **506** is removed prior to forming the spacers **508'**. As discussed above, the insulating layer **501** (such as a silicon oxide and/or silicon oxynitride layer) and the etch stopping layer **503** (such as a silicon nitride layer) may be formed on substrate **500**, and the conductive plugs **502** (such as polysilicon plugs) may be formed in holes through the insulating and etch stop layers **501** and **503**.

[0058] The first sacrificial layer **504** (such as a layer of silicon oxide and/or silicon oxynitride) may then be formed on the etch stop layer **503** (to a thickness greater than that illustrated in Figure 4A), and holes in the first sacrificial layer **504** may expose the conductive plugs **502**. A conductive layer (such as a polysilicon layer) may be formed on the first sacrificial layer **504** and on sidewalls of the holes therein, and the second sacrificial layer **506** may be formed on the conductive layer to a thickness greater than that illustrated in Figure 2A. The second sacrificial layer **506** and the conductive layer may then be etched and/or polished back to expose the first sacrificial layer **504** and so that portions of the conductive layer remaining in the holes define electrically isolated electrodes **505'**.

[0059] After exposing the first sacrificial layer **504**, portions of the first and second sacrificial layers **504** and **506** may be selectively removed (with respect

to the electrodes 505'), for example, using a buffered oxide etch such as a LAL chemical etch discussed above. Accordingly, portions of the electrodes 505' may be protected by remaining portions of the sacrificial layers 504 and 506 and portions of the electrodes 505' may be exposed. According to embodiments of Figures 4A-B, a length of exposed portions of the electrodes 505' may be greater than a length of exposed portions of the electrodes 205' of Figures 2C-E.

[0060] A layer of an insulating material (such as silicon nitride) may be formed on exposed portions of the electrodes 505' and on remaining portions of the sacrificial layers 504 and 506. The layer of the insulating material may then be subjected to an anisotropic etch to provide the spacers 508' shown in Figure 4A. As compared to forming the spacers 208' as discussed above with respect to Figures 2D-E, a greater etch depth/time may be used to form the spacers of Figure 4A so that portions of the electrodes 505' extending beyond the sacrificial layers 504 and 506 and beyond the spacers 508' are exposed.

[0061] Once the spacers 508' have been formed, the sacrificial layers 504 and 506 can be removed as shown in Figure 4B. The sacrificial layers may be removed, for example, using a buffered oxide etch such as an LAL chemical etch as discussed above. A capacitor dielectric layer may then be formed on exposed portions of the electrodes 505', and a second capacitor electrode may be formed on the capacitor dielectric layer opposite the electrodes 505'. Relatively long electrodes may be subject to bowing/bending so that electrical contact/shorting therebetween may occur at intermediate portions of the electrodes in addition to or instead of at ends thereof. By placing the spacers at intermediate positions along the electrodes 505', contact between electrodes due to bowing may be reduced. According to embodiments illustrated in Figures 4A-B, electrode walls of increased length may be accommodated without electrical shorts therebetween to increase an electrode surface area.

[0062] Steps of forming electrodes according to yet additional embodiments of the present invention are illustrated in Figures 5A-B. The structure illustrated in Figure 5A can be formed according to steps similar to those discussed above with respect to Figures 3A-B, with a difference being that a

greater thickness of the sacrificial layers **604** and **606** is removed prior to forming recessed portions of the electrode walls and forming the spacers **608'**. As discussed above, the insulating layer **601** (such as a silicon oxide and/or silicon oxynitride layer) and the etch stopping layer **603** (such as a silicon nitride layer) may be formed on substrate **600**, and the conductive plugs **602** (such as polysilicon plugs) may be formed in holes through the insulating and etch stop layers **601** and **603**.

[0063] The first sacrificial layer **604** (such as a layer of silicon oxide and/or silicon oxynitride) may then be formed on the etch stop layer **603** (to a thickness greater than that illustrated in Figure 5A), and holes in the first sacrificial layer **604** may expose the conductive plugs **602**. A conductive layer (such as a polysilicon layer having a thickness of approximately 500\AA) may be formed on the first sacrificial layer **604** and on sidewalls of the holes therein, and the second sacrificial layer **606** may be formed on the conductive layer to a thickness greater than that illustrated in Figure 3A. The second sacrificial layer **606** and the conductive layer may then be etched and/or polished back to expose the first sacrificial layer **604** and so that portions of the conductive layer remaining in the holes define electrically isolated electrodes **605'** as shown in Figure 5A.

[0064] After exposing the first sacrificial layer **604**, portions of the first and second sacrificial layers **604** and **606** may be selectively removed (with respect to the electrodes **605'**), for example, using a buffered oxide etch such as a LAL chemical etch discussed above. Accordingly, portions of the electrodes **605'** may be protected by remaining portions of the sacrificial layers **604** and **606** and portions of the electrodes **605'** may be exposed. According to embodiments of Figures 5A-B, a length of exposed portions of the electrodes **605'** may be greater than a length of exposed portions of the electrodes **305'** of Figures 3C-E.

[0065] Portions of the electrode wall inside and outside surfaces exposed by the sacrificial layers **604** and **606** may then be etched to provide recessed portions of the electrode walls. For example, an isotropic etch may be used that removes the conductive material of the electrodes **605'** selectively with respect to the first and second sacrificial layers **604** and **606**. More particularly,

approximately 150Å of the exposed portions of the electrodes may be removed so that exposed portions of the electrodes 605' are recessed with respect to portions of the electrode 605' protected by the sacrificial layers 604 and 606. Portions of the electrodes 605' protected by the sacrificial layers 604 and 606 may thus maintain a thickness of approximately 500Å while portions of the electrodes 605' extending beyond the sacrificial layers 604 and 606 may be thinned to approximately 200Å, as shown in Figure 5A.

[0066] A layer of an insulating material (such as silicon nitride) may be formed on exposed portions of the electrodes 605' and on remaining portions of the sacrificial layers 604 and 606. The layer of the insulating material may then be subjected to an anisotropic etch to provide the spacers 608' shown in Figure 5A. As compared to forming the spacers 608' as discussed above with respect to Figures 3D-E, a greater etch depth/time may be used to form the spacers of Figure 5A so that portions of the electrodes 605' extending beyond the sacrificial layers 604 and 606 and beyond the spacers 608' are exposed.

[0067] Once the spacers 608' have been formed, the sacrificial layers 604 and 606 can be removed as shown in Figure 5B. The sacrificial layers may be removed, for example, using a buffered oxide etch such as an LAL chemical etch as discussed above. A capacitor dielectric layer may then be formed on exposed portions of the electrodes 605', and a second capacitor electrode may be formed on the capacitor dielectric layer opposite the electrodes 605'. Relatively long electrodes may be subject to bowing/bending so that electrical contact/shorting therebetween may occur at intermediate portions of the electrodes in addition to or instead of at ends thereof. By placing the spacers at intermediate positions along the electrodes 605', electrical contact between electrodes due to bowing may be reduced. According to embodiments illustrated in Figures 5A-B, electrode walls of increased length may be accommodated without electrical shorts therebetween to increase an electrode surface area. Moreover, by providing the spacers on recessed portions of the electrodes, shadowing of portions of the electrodes (between the spacers and the substrate) can be reduced during subsequent depositions. Accordingly, uniformity of a capacitor dielectric layer formed on the capacitor

electrodes may be improved. Stated in other words, by reducing an overhang of the spacers, a shadowing of portions of the electrodes between the spacers and the substrate can be reduced.

[0068] While this invention has been particularly shown and described with reference to preferred embodiments thereof, it will be understood by those skilled in the art that various changes in form and details may be made therein without departing from the spirit and scope of the invention as defined by the appended claims.